REMARKS

Claim Rejections

Claims 14-17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 14-15 and 17 are rejected under 35 U.S.C. 103(a). Claim 16 is also separately rejected under 35 U.S.C. 103(a).

Amended Claims

By this Amendment, Applicant has amended claims 14-16 of this application to include element numbers and additional amendments to render the claims more definite in order to overcome the Examiner's rejections under 35 U.S.C. §112, second paragraph. It is believed that the amended claims specifically set forth each element of Applicant's invention in full compliance with 35 U.S.C. § 112, and define subject matter that is patentably distinguishable over the cited prior art, taken individually or in combination.

Applicant's amended claims are directed toward: a method of forming a 8-layer printed circuit board (PCB) comprising the steps of:

preparing a core 1 including a thin compound plate having an inner layer 101 made of a prepreg material and two copper clad layers 102 provided on two outer sides of the inner layer; (see Fig. 2A)

performing a circuit formation on the two copper clad layers (102) forming part of the core (1) by way of etching to form two circuit layers (1a, 1b) on the two outer sides of the inner layer, respectively;(see Fig. 2B)

laminating a dielectric layer to form a laminated dielectric layer (2) from the prepreg material and a copper clad layer (3) are sequentially formed on each of the two circuit layer (1a, 1b), so that a four-layer PCB is formed; (see Fig. 2C)

forming another two circuit layers (3a, 3b) on the copper clad layers (3) to form the another two circuit layers (3a, 3b) on outer sides of the two dielectric layers (2); (see Fig. 2D)

forming two resin layers 4 being separately formed with a resin build-up process through liquid epoxy coating or dry film type epoxy laminating on the two

circuit layers 3a,3b by way of applying a dielectric material and epoxy on outer sides of two circuit layers 3a, 3b; (see Fig. 2E)

forming necessary conductive holes 4a,4b on the resin layers 4 by performing laser drilling and mechanical drilling, respectively, to form a PCB; (see Fig. 2F)

plating the PCB with copper to form a copper-plating layer 5 on all outer surfaces of the PCB ; (see Fig. 2G)

performing the circuit formation by way of etching the copper- plating layer 5 to form two additional circuit layers; (see Fig. 2H)

and

forming another two laminating dielectric layers 6 from the prepreg material, and another two copper clad layers 7 being sequentially formed on outer sides of the two additional circuit layers 5a, 5b by way of lamination to form the 8-layer PCB, (see Fig.2I)

wherein the 8-layer PCB has only 8 layers.

In response to the Examiner's comments on p. 6 of the outstanding Office Action, Applicant now notes that the claims have been recited to specify that the PCB has only 8 layers. It follows that Applicant's arguments of 2/22/08, which are maintained and incorporated by reference, are fully applicable to the pending claims.

Referring to the structure of the "8-layer printed circuit board (PCB) 100" disclosed in the above-mentioned claims of the present invention , (see page 13, line 1-17 of the specification), the circuit layers 7a and 7b shall be referred to as the outer circuit layers that form a first layer of the PCB 100, while the circuit layers 1a and 1b, 3a and 3b, and 5a and 5b shall be referred to as the inner circuit layers. Wherein, the inner circuit layers 5a and 5b and the inner circuit layers 3a and 3b form a second and a third layer, respectively, of the PCB 100, and are also referred to as the second and the third inner circuit layer, respectively, hereinafter.

Furthermore, see page 13, line 19 to page 15, line 7 of the specification which teaches that the present invention is characterized in that the resin build-up process and the lamination process are employed to form the inner circuit layers and the outer circuit layers, respectively, of the 8-layer PCB 100. More specifically, the inner circuit layers, such as the second inner circuit layers 5a and 5b, which require refinement of circuits are formed by using a resin material, such as epoxy, as the

dielectric to form the resin layers 4 with the resin build-up process through liquid epoxy coating or dry film type epoxy laminating, and then forming the inner circuit layers 5a and 5b. Thereafter, the dielectric layers 6 using the prepreg or the aramid fiber material as the dielectric and the outer circuit layers 7a, 7b are formed with the lamination process. By using the resin build-up process and the lamination process to form different layers on the same one multi-layer PCB, the completed multi-layer PCB 100 is able to include advantages obtainable from the two processes. For example, the second inner circuit layers 5a and 5b of the multi-layer PCB 100 formed with the resin build-up process have upgraded circuit refinement to satisfy the circuit design requirement of the multi-layer PCB, and the outer circuit layers 7a and 7b of the multi-layer PCB 100 formed with the lamination process have improved thermal resistance, copper peel strength, stiffness, thermal stress reliability, and size stability. Therefore, the fully completed 8-layer PCB 100 has a quality reliability superior to that of a multi-layer PCB formed with only one of the conventional forming processes. Moreover, since at least some of the inner circuit layers, for example, the second inner circuit layers 5a and 5b, use resin layers 4 as the dielectric layers, and the cost for the resin material is much lower than the cost for the prepreg or the aramid fiber material used as the laminating dielectric layers 6, the multi-layer PCB made according to the method of the present invention has reduced material cost to lower the overall manufacturing cost thereof.

Depending on the above-mentioned distinguishing features and the serial forming steps in sequence (in order) as shown in Fig.2A-2I respectively of the present invention, Applicant believes that the present invention is obviously different from the Cited References: Peterson et al (US 4,882,454), Kiyota et al (US 5,263,248), Haba et al (US 6,675,469), Cutting et al (US 5,638,597) and Shin et al (US 6,405,431).

Furthermore, the pending claim 14 of the present invention recites a particular method of forming a particular 8-layer printed circuit board (PCB), especially a serial forming steps in sequence as shown in Fig.2A-2I respectively. Therefore the distinguishing features and advantages of the present invention at least include:

1) The resin build-up process and the lamination process are employed to form the inner circuit layers and the outer circuit layers, respectively, of the 8-layer

PCB 100. The second inner circuit layers 5a and 5b, which require refinement of circuits are formed by using a resin material, such as epoxy, as the dielectric to form the resin layers 4 with the resin build-up process through liquid epoxy coating or dry film type epoxy laminating, and then forming the inner circuit layers 5a and 5b. Thereafter, the dielectric layers 6 using the prepreg or the aramid fiber material as the dielectric and the outer circuit layers 7a, 7b are formed with the lamination process.

2) By using the resin build-up process and the lamination process to form different layers on the same one multi-layer PCB, the completed multi-layer PCB 100 is able to include advantages obtainable from the two processes. The second inner circuit layers 5a and 5b of the multi-layer PCB 100 formed with the resin build-up process have upgraded circuit refinement to satisfy the circuit design requirement of the multi-layer PCB, and the outer circuit layers 7a and 7b of the multi-layer PCB 100 formed with the lamination process have improved thermal resistance, copper peel strength, stiffness, thermal stress reliability, and size stability.

3) The reliability of the fully completed 8-layer PCB 100 formed by utilizing the particular method with a serial forming steps in sequence as shown in Fig.2A-2I respectively is superior to that of a multi-layer PCB formed with only one of the conventional forming processes.

4) The multi-layer PCB 100 made according to the method of the present invention has reduced material cost to lower the overall manufacturing cost thereof. The second inner circuit layers 5a and 5b use resin layers 4 as the dielectric layers, and the cost for the resin material is much lower than the cost for the prepreg or the aramid fiber material used as the laminating dielectric layers 6.

Although the Cited References: Peterson et al (US 4,882,454), Kiyota et al (US 5,263,248), Haba et al (US 6,675,469), Cutting et al (US 5,638,597) and Shin et al (US 6,405,431) teach multi-layer PCBs, each of the Cited References discloses only a pair of a multi-layer PCB structure or a portion of forming steps of forming a multi-layer PCB. Thus each of the Cited References should be considered as a multi-layer PCB formed with only one of the conventional forming processes as mentioned in " BACKGROUND" of the present invention. The foregoing means each of the Cited References do not disclose the distinguishing features and the serial

forming steps in sequence as shown in Fig.2A-2I of the present invention (and recited in claim 14) and therefore is impossible to have or achieve the above-mentioned functional advantages and effect of the present invention.

4) In summary, claim 14 of the present invention recites a particular method of forming a particular 8-layer printed circuit board (PCB)100, especially the serial forming steps in sequence as shown in Fig.2A-2I (and recited in claim 14). As a result, the Cited References does not disclose the distinguishing features and the serial forming steps in sequence as shown in Fig.2A-2I and does not have or achieve the functional advantages and effect of the present invention.

It follows that even if the teachings of Peterson et al (US 4,882,454), Kiyota et al (US 5,263,248), Haba et al (US 6,675,469), Cutting et al (US 5,638,597) and Shin et al (US 6,405,431) were combined, as suggested by the Examiner, the resultant combination does not reasonably teach: a method of forming a 8-layer printed circuit board (PCB) comprising the steps of: preparing a core 1 including a thin compound plate having an inner layer 101 made of a prepreg material and two copper clad layers 102 provided on two outer sides of the inner layer; performing a circuit formation on the two copper clad layers (102) forming part of the core (1) by way of etching to form two circuit layers (1a, 1b) on the two outer sides of the inner layer, respectively; laminating a dielectric layer to form a laminated dielectric layer (2) from the prepreg material and a copper clad layer (3) are sequentially formed on each of the two circuit layer (1a, 1b), so that a four-layer PCB is formed; forming another two circuit layers (3a, 3b) on the copper clad layers (3) to form the another two circuit layers (3a, 3b) on outer sides of the two dielectric layers (2); forming two resin layers 4 being separately formed with a resin build-up process through liquid epoxy coating or dry film type epoxy laminating on the two circuit layers 3a,3b by way of applying a dielectric material and epoxy on outer sides of two circuit layers 3a, 3b; forming necessary conductive holes 4a,4b on the resin layers 4 by performing laser drilling and mechanical drilling, respectively, to form a PCB; plating the PCB with copper to form a copper-plating layer 5 on all outer surfaces of the PCB ; performing the circuit formation by way of etching the copper- plating layer 5 to form two additional circuit layers; and forming another two laminating dielectric layers 6 from the prepreg material, and another two copper clad layers 7 being

sequentially formed on outer sides of the two additional circuit layers 5a, 5b by way of lamination to form the 8-layer PCB, wherein the 8-layer PCB has only 8 layers.

It is a basic principle of U.S. patent law that it is improper to arbitrarily pick and choose prior art patents and combine selected portions of the selected patents on the basis of Applicant's disclosure to create a hypothetical combination which allegedly renders a claim obvious. The Supreme Court, in *KSR International Co. v. Teleflex Inc. et al.*, 550 U.S. 1, 82 USPQ2d at 1391 (2007), reaffirmed the framework of *Graham* v. *John Deere Co. of Kansas City* for determining obviousness under 35 U.S.C. 103. In that decision, the Supreme Court stated, at page 2:

> In *Graham* v. *John Deere Co. of Kansas City*, 383 U. S. 1 (1966), the Court set out a framework for applying the statutory language of §103, language itself based on the logic of the earlier decision in *Hotchkiss* v. *Greenwood*, 11 How. 248 (1851), and its progeny. See 383 U. S., at 15–17. The analysis is objective:
>
> > "Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." *Id.*, at 17–18.

> While the sequence of these questions might be reordered in any particular case, the factors continue to define the inquiry that controls. If a court, or patent examiner, conducts this analysis and concludes the claimed subject matter was obvious, the claim is invalid under §103.

The Supreme Court, in *KSR International Co. v. Teleflex*, 550 U.S. at 14, 82 USPQ2d at 1396, explained that:

> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicit. See In re Kahn, 441 F. 3d 977, 988 (CA Fed. 2006) (***"[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness"***). Emphasis Added

Applicant submits that the above-presented arguments clearly indicate that the Examiner has failed to provide an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" for combining selected elements of Peterson et al (US 4,882,454) with selected elements of Kiyota et al (US 5,263,248), Haba et al (US 6,675,469), Cutting et al (US 5,638,597) and Shin et al (US 6,405,431). *KSR* at 1396 *(*citing *In re Kahn* at 988). Clearly, such a combination is not an acceptable combination under 35 U.S.C. §103. The rejections of Applicant's claims as being rendered by the aforementioned combinations of references under 35 U.S.C. §103 are respectfully traversed.

Summary

In view of the foregoing amendments and remarks, Applicant submits that this application is now in condition for allowance and such action is respectfully requested. Should any points remain in issue, which the Examiner feels could best be resolved by either a personal or a telephone interview, it is urged that Applicant's local attorney be contacted at the exchange listed below.

Respectfully submitted,

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